Attorney Docket: 012.P10010

AMENDMENT

IN THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the current application. Please amend the claims as follows:

1. (Previously Presented) A method, comprising:

storing in a memory a first phasor associated with an electronic signal and a second phasor generated by multiplying together the first phasor with a delta phasor associated with a cyclic rate of the electronic signal, the first phasor having a first real portion and a first imaginary portion, the second phasor having a second real portion and a second imaginary portion;

storing in the memory a first sum generated by adding the first imaginary portion to the first real portion;

generating an imaginary correction factor by scaling the first sum according to a first scaling factor;

correcting a magnitude error of the second phasor by adding the imaginary correction factor to the second imaginary portion of the second phasor; and

updating the electronic signal based on the corrected second phasor.

2. (Previously Presented) The method of claim 1, further comprising:

storing in the memory a first difference generated by subtracting the first imaginary portion from the first real portion;

scaling the first difference according to the first scaling factor to produce a real correction factor; and

further correcting the magnitude error of the second phasor by adding the real correction factor to the second real portion of the second phasor.

3. (Previously Presented) The method of claim 1, wherein the first scaling factor is based on a bit-precision of N bits, where N is a non-zero integer.

4. (Amended) The method of claim 3, wherein the first ~~correction~~ scaling factor is further based on a second ~~correction~~ scaling factor, the second ~~correction~~ scaling factor being based on a first term of a Taylor series relating to a square-root.

5. (Previously Presented) The method of claim 4, wherein the second scaling factor is based on the formula:

$$\alpha = \left(\frac{1.0 - \left(\cos^2(\omega) + \sin^2(\omega) \right)}{2} \right)$$

where α is the second scaling factor and ω is the frequency of the complex sinusoid.

6. (Amended) The method of claim 5, wherein the second ~~correction~~ scaling factor is determined according to the formula $\alpha \approx 2^{-P}$, where P is a non-zero integer.

7. (Previously Presented) The method of claim 6, wherein the first scaling factor is equal to $2^{-(P+N)}$.

8. (Previously Presented) The method of claim 7, wherein the step of scaling is performed using a shift operation.

9. (Previously Presented) The method of claim 1, wherein the step of scaling is performed using a shift operation.

10. (Previously Presented) The method of claim 1, further comprising updating the electronic signal based on a third phasor produced a high-accuracy technique.

11. (Previously Presented) The method of claim 1, wherein the electronic signal is an electronic analog signal having sinusoidal form.

12. (Previously Presented) The method of claim 1, further comprising producing a communication signal based on the updated electronic signal.

13. (Previously Presented) The method of claim 1, further comprising receiving a communication signal using the updated electronic signal.

14. (Previously Presented) The method of claim 2, wherein the steps of scaling are performed using a shift operation of N+P bits, where N is a target bit-precision and P is a non-zero integer such that

$$2^{-P} \approx \left(\frac{1.0-\left(\cos^2(\omega)+\sin^2(\omega)\right)}{2}\right)$$

where ω is the frequency of the complex sinusoid.

15. (Previously Presented) An apparatus for producing an electronic signal, comprising:

a multiplier that multiplies a first phasor associated with the electronic signal and a delta phasor associated with a cyclic rate of the electronic signal to produce a second phasor, the first phasor having a first real portion and a first imaginary portion, the second phasor having a second real portion and a second imaginary portion;

an arithmetic device that adds the first imaginary portion to the first real portion to produce a first sum;

a scaling device that scales the first sum according to a first scaling factor to produce an imaginary correction factor;

an adding device that adds the imaginary correction factor to the second imaginary portion of the second phasor to correct for a magnitude error of the second phasor; and

an interface that updates the electronic signal based on the corrected second phasor.

16. (Previously Presented) The method of claim 15, wherein the electronic signal is an electronic analog signal having sinusoidal form.

17. (Previously Presented) The method of claim 15, wherein the electronic signal is a communication signal having embedded information.

18. (Previously Presented) The apparatus of claim 15, wherein the arithmetic device further subtracts the first imaginary portion from the first real portion to produce a first difference, the scaling device further scales the first difference according to the first scaling factor to produce a real correction factor; and the adding device further adds the real correction factor to the second real portion of the second phasor to further correct for the magnitude error of the second phasor.

19. (Previously Presented) The apparatus of claim 15, wherein the first scaling factor is based on a bit-precision of N bits, where N is a non-zero integer.

20. (Amended) The apparatus of claim 15, wherein the first ~~correction~~ scaling factor is further based on a second ~~correction~~ scaling factor, the second ~~correction~~ scaling factor being based on a first term of a Taylor series.

21. (Previously Presented) The apparatus of claim 16, wherein the second scaling factor is based on the formula:

$$\alpha = \left(\frac{1.0 - \left(\cos^2(\omega) + \sin^2(\omega)\right)}{2}\right)$$

where α is the second scaling factor and ω is the frequency of the complex sinusoid.

22. (Amended) The apparatus of claim 21, wherein the second ~~correction~~ scaling factor is determined according to the formula $\alpha = 2^{-P}$, where P is a non-zero integer.

23. (Previously Presented) The apparatus of claim 22, wherein the scaling device scales the first sum device using a shift operation.

24. (Previously Presented) The apparatus of claim 15, wherein the scaling device scales the first sum device using a shift operation.

25. (Previously Presented) The apparatus of claim 15, wherein the apparatus further updates the electronic signal based on a third phasor, the third phasor being produced a high-accuracy technique.

26. (Previously Presented) A machine-readable medium including instructions for producing an electronic signal, the instructions being arranged to cause a machine to perform the steps of:

multiplying a first phasor associated with the electronic signal and a delta phasor associated with a cyclic rate of the electronic signal to produce a second phasor, the first phasor having a first real portion and a first imaginary portion, the second phasor having a second real portion and a second imaginary portion;

adding the first imaginary portion to the first real portion to produce a first sum;

scaling the first sum according to a first scaling factor to produce an imaginary correction factor;

adding the imaginary correction factor to the second imaginary portion of the second phasor to correct for a magnitude error of the second phasor; and

updating the electronic signal based on the corrected second complex sinusoid phasor.

27. (Previously Presented) The machine-readable medium of claim 26, further comprising instructions being arranged to cause a machine to perform the steps of:

subtracting the first imaginary portion from the first real portion to produce a first difference;

scaling the first difference according to the first scaling factor to produce a real correction factor; and

adding the real correction factor to the second real portion of the second phasor to further correct for the magnitude error of the second phasor.

28. (Previously Presented) The machine-readable medium of claim 27, wherein the steps of scaling are performed using a shift operation of N+P bits, where N is a target bit-precision and P is a non-zero integer such that

$$2^{-P} \approx \left(\frac{1.0 - \left(\cos^2(\omega) + \sin^2(\omega) \right)}{2} \right)$$

where ω is the frequency of the complex sinusoid.

29. (Previously Presented) An apparatus for producing an electronic signal, comprising:

a multiplying means for multiplying a first phasor associated with the electronic signal and a delta phasor associated with a cyclic rate of the electronic signal to produce a second

phasor, the first phasor having a first real portion and a first imaginary portion, the second phasor having a second real portion and a second imaginary portion;

an arithmetic means for adding the first imaginary portion to the first real portion to produce a first sum;

a scaling means for scaling the first sum according to a first scaling factor to produce an imaginary correction factor;

an adding means for adding the imaginary correction factor to the second imaginary portion of the second phasor to correct for a magnitude error of the second phasor;

an interface that updates the electronic signal based on the corrected second phasor.

30. (Previously Presented) The apparatus of claim 29, wherein the arithmetic means further subtracts the first imaginary portion from the first real portion to produce a first difference, the scaling means further scales the first difference according to the first scaling factor to produce a real correction factor; and the adding means further adds the real correction factor to the second real portion of the second phasor to further correct for the magnitude error of the second phasor.

31. (Previously Presented) The apparatus of claim 29, wherein the scaling means performs its scaling without using a multiply operation.

32. (Previously Presented) The apparatus of claim 29, wherein the scaling means performs its scaling using one or more shift operations.

33. (Previously Presented) The apparatus of claim 29, further comprising a communication-based device that produces a communication signal using the updated electronic signal.

34. (Previously Presented) The apparatus of claim 29, further comprising a communication-based device that receives a communication signal using the updated electronic signal.

35. (New) A method, comprising:

combining a first phasor associated with an electronic signal and a delta phasor associated with a cyclic rate of the electronic signal to produce a second phasor;

adding a first correction factor to the second phasor to provide a corrected second phasor; and

updating the electronic signal based at least in part on the corrected second phasor.

36. (New) The method of claim 35, wherein the first phasor comprises a first real component and a first imaginary component, and the second phasor has a second real component and a second imaginary component.

37. (New) The method of claim 36, wherein the first correction factor is substantially formed by adding the first imaginary portion to the first real portion to produce a first sum, and scaling the first sum according to a first scaling factor to produce the first correction factor.

38. (New) The method of claim 37, wherein providing a corrected second phasor further comprises:

adding the first correction factor to the second imaginary portion of the second phasor to correct for a magnitude error of the second phasor.

39. (New) The method of claim 37, further comprising:

subtracting the first imaginary portion from the first real portion to produce a first difference;

scaling the first difference according to the first scaling factor to produce a second correction factor; and

adding the second correction factor to the second real portion of the second phasor to further correct for the magnitude error of the second phasor.

40. (New) The method of claim 39, wherein the first scaling factor is further based on a second scaling factor, the second scaling factor being based on a first term of a Taylor series relating to a square-root.

41. (New) The method of claim 40, wherein the second scaling factor is based on the formula:

$$\alpha = \left(\frac{1.0 - \left(\cos^2(\omega) + \sin^2(\omega) \right)}{2} \right)$$

where α is the second scaling factor and ω is the frequency of a complex sinusoid.

42. (New) The method of claim 41, wherein the second scaling factor is determined according to the formula $\alpha \approx 2^{-P}$, where P is a non-zero integer.

43. (New) The method of claim 37, wherein the first scaling factor is equal to $2^{-(P+N)}$.

44. (New) The method of claim 39, wherein the scaling is performed using a shift operation.

45. (New) The method of claim 35, further comprising updating the electronic signal based, at least in part, on a third phasor.

46. (New) The method of claim 35, further comprising producing a communication signal based on the updated electronic signal.

47. (New) The method of claim 39, wherein the scaling comprises shifting a binary representation of a first sum of N+P bits, where N is a target bit-precision and P is a non-zero integer such that

$$2^{-P} \approx \left(\frac{1.0-\left(\cos^2(\omega)+\sin^2(\omega)\right)}{2}\right)$$

where ω is the frequency of a complex sinusoid.

48. (New) A system, comprising:

circuitry to combine a first phasor associated with an electronic signal and a delta phasor associated with a cyclic rate of the electronic signal to produce a second phasor;

circuitry to produce a correction factor;

circuitry to add the correction factor to the second phasor to correct for a magnitude error of the second phasor; and

circuitry to update the electronic signal based, at least in part, on the corrected second phasor.

49. (New) The system of claim 48, wherein the first phasor comprises a first real component and a first imaginary component, the second phasor comprises a second real component and a second imaginary component.

50. (New) The system of claim 48, wherein the electronic signal is a communication signal.

51. (New) The system of claim 49, and further comprising circuitry to subtract the first imaginary component from the first real component to produce a first difference;

scale the first difference according to a first scaling factor to produce a real correction factor; and

add the real correction factor to the second real portion of the second phasor to correct for the magnitude error of the second phasor.

52. (New) The system of claim 52, wherein the first scaling factor is based, at least in part, on a bit-precision of N bits, where N is a non-zero integer.

53. (New) The system of claim 51, wherein the first scaling factor is further based, at least in part, on a second scaling factor, the second scaling factor being based on a first term of a Taylor series.

54. (New) The system of claim 53, wherein the second scaling factor is based at least in part on the formula:

$$\alpha = \left(\frac{1.0 - \left(\cos^2(\omega) + \sin^2(\omega)\right)}{2} \right)$$

where α is the second scaling factor and ω is the frequency of the complex sinusoid.

55. (New) The system of claim 53, wherein the second scaling factor is determined according to the formula $\alpha = 2^{-P}$, where P is a non-zero integer.

56. (New) The system of claim 48, and further comprising circuitry to update the electronic signal based at least in part on a third phasor.

57. (New) An article comprising: a storage medium having stored thereon instructions that if executed by a computing device performs a method as follows:

combining a first phasor associated with an electronic signal and a delta phasor associated with a cyclic rate of the electronic signal to produce a second phasor;

adding a first correction factor to the second phasor to provide a corrected second phasor; and

updating the electronic signal based at least in part on the corrected second phasor.

58. (New) The article of claim 57, wherein the first phasor comprises a first real component and a first imaginary component, and the second phasor has a second real component and a second imaginary component.

59. (New) The method of claim 58, wherein the instructions, if further executed, produce a correction factor as follows:

adding the first imaginary portion to the first real portion to produce a first sum;

scaling the first sum according to a first scaling factor to produce a first correction factor;

adding the first correction factor to the second imaginary portion of the second phasor to correct for a magnitude error of the second phasor.

60. (New) The method of claim 59, wherein the instructions, if further executed, perform a method comprising:

subtracting the first imaginary portion from the first real portion to produce a first difference;

scaling the first difference according to the first scaling factor to produce a second correction factor; and

adding the second correction factor to the second real portion of the second phasor to further correct for the magnitude error of the second phasor.

61. (New) The article of claim 60, wherein the first scaling factor is further based on a second scaling factor, the second scaling factor being based on a first term of a Taylor series relating to a square-root.

62. (New) The article of claim 61, wherein the second scaling factor is based on the formula:

$$\alpha = \left(\frac{1.0 - \left(\cos^2(\omega) + \sin^2(\omega)\right)}{2}\right)$$

where α is the second scaling factor and ω is the frequency of a complex sinusoid.

63. (New) The article of claim 61, wherein the second scaling factor is determined according to the formula $\alpha \approx 2^{-P}$, where P is a non-zero integer.

64. (New) The article of claim 59, wherein the first scaling factor is equal to $2^{-(P+N)}$.

65. (New) The article of claim 59, wherein the scaling is performed using a shift operation of N+P bits, where N is a target bit-precision and P is a non-zero integer such that

$$2^{-P} \approx \left(\frac{1.0 - \left(\cos^2(\omega) + \sin^2(\omega)\right)}{2}\right)$$

where ω is the frequency of a complex sinusoid.